REMARKS/ARGUMENTS

Claims 1-13 are currently pending in the present patent application.

In the Office Action mailed September 21, 2005, the Examiner objected to Figure 5 as including "reference character(s) not mentioned in the description: a delay, a divider, and a D Flip-flop as shown in Fig. 5." The undersigned cannot find anywhere in Title 37 of the Code of Federal Regulations, specifically Rules 81, 83, 84, and 85 directed to drawings, where the rules require that every component illustrated in a figure be assigned a reference character and described in the specification. Regardless, paragraph 27 has been amended through the above amendments to include an express description of the delay, divider, and D-type flip-flop illustrated in Figure 5. Figure 5 has similarly been amended through the accompanying drawing amendment to assign reference numbers to these components. No new matter has been introduced through any of these amendments.

The Examiner also rejected claim 3 under Section 112, first paragraph, as failing to comply with the enablement requirement for containing subject matter not described in the specification in a way to enable a person skilled in the art to make or use the invention. Specifically, the Examiner points to the "predictor and corrector" and "output generator" elements recited in claim 3 as not being enabled in the specification. Figure 2 clearly shows these elements and paragraph 20 explains the interconnection and general function of each. The process flow diagram of Figure 3 illustrates in more detail an example process flow for the predictor and corrector 18 shown in Figure 2.

Figure 5 illustrates another embodiment of the frequency synthesizer 14 and the operation of this embodiment is described in paragraph 23 *et seq.* In the embodiment of Figure 5, the second synchronizer 26 receives the dithered signal Fdither but only when enable signal is active will the second synchronizer be enabled and reset the edge counter 32 and expected count latch 30. Thus, the synchronizer 26 clears the counter 32 and latch 30 in response to being clocked by the Fdither signal only when enabled. The enable signal goes active so that the synchronizer 26 resets the counter 32 and latch 30 responsive to the Fdither signal to thereby clear or reset these counter. Thereafter, the enable signal goes inactive so that the counter 32 and latch 30 function as desired during normal operation of the frequency synthesizer 14.

From the above comments, one skilled in the art will understand the operation of the

embodiment of Figure 5 in conjunction with the associated description and thus the subject matter of claim 3 is enabled and claim satisfies paragraph one of Section 112. These same comments apply to the Examiner's rejections of claims 4-6 and 8-13. Furthermore, with regard to the "selecting a desired number of periods in the dithered signal" element of claim 3, the process flow diagram of Figure 7 and paragraph 31 expressly indicates that the "[i]n step 320, the desired number of [high frequency] HF [or dithered] clocks per sample register is determined via the configuration registers." Thus, values stored in the configuration registers select this value. The description in paragraph 31 also enables the "determining an average number of fractional of dithered periods" operation recited in claim 9. These same comments, along with the description of paragraph 32, apply to the rejection of claim 13 under Section 112, first paragraph. Claim 7 has been amended to eliminate any antecedent basis problems under the second paragraph of Section 112.

The Examiner further rejected claims 1 and 2 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,719,512 to Murayama ("Murayama"). The Examiner points to Figure 6 of Murayama for disclosing all elements recited in claims 1 and 2.

Claim 1 recites a circuit including a reference signal, a frequency synthesizer receiving a dithered signal and the reference signal and generating a constant frequency output, and configuration registers transceiving data and control signals with the frequency synthesizer.

Murayama neither discloses nor suggests a circuit as recited in claim 1. The Murayama patent is directed to a circuit for extracting the color burst sinusoid, both frequency and phase, for an NTSC/PAL/SECAM composite video signal using a reference crystal. This color burst clock is extracted from the exact but intermittent color burst from the composite video signal. In contrast, with the circuit of claim 1 a relatively stable clock in the form of the constant frequency output is generated from an arbitrary high-frequency spread-spectrum input clock in the form of the dithered signal and from a fixed reference clock signal. The Murayama patent extracts the color clock from the exact but intermittent color burst from the composite video signal. Murayama utilizes an incoming frequency controlled clock while in the circuit of claim 1 the dithered signal is varying and thus is not an incoming frequency controlled clock. The constant frequency output of claim 1 is based upon the fixed frequency reference clock signal as described in the specification, and thus this reference signal is a lower fixed frequency reference clock signal as this term is utilized

in claim 1. The signal 22 in Murayama is a burst signal obtained from a composite video signal and is not a reference signal as recited in claim 1. The reference signal as recited in claim 1 is a fixed reference frequency having a lower frequency than the high speed dithered clock signal, with the fixed reference frequency being utilized to remove clock edges to obtain the desired constant frequency output.

For these reasons, Murayama neither discloses nor suggest the circuit recited in claim 1 and the combination of elements recited in claim 1 is accordingly allowable. Dependent claims 2-7 are allowable for at least the same reasons as claim 1 and due to the additional limitation added by these claims. The remaining claims, while not rejected in the Office Action as being anticipated by Murayama, are allowable for similar reasons.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to resolve the matter. If any need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

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